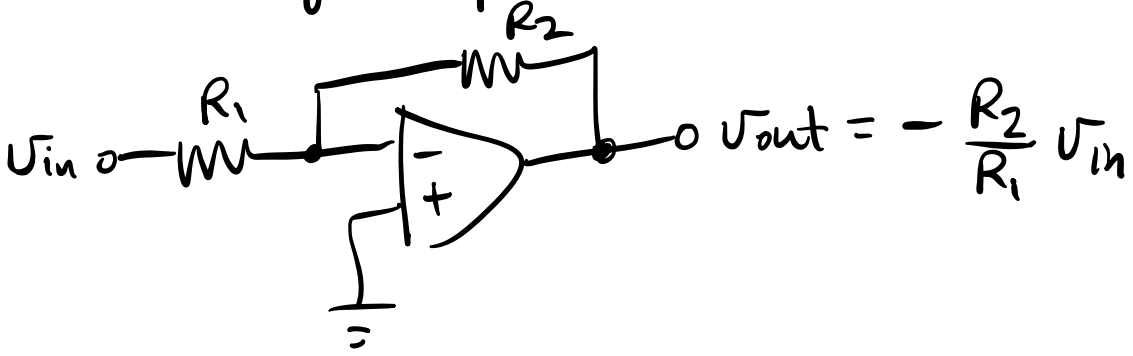
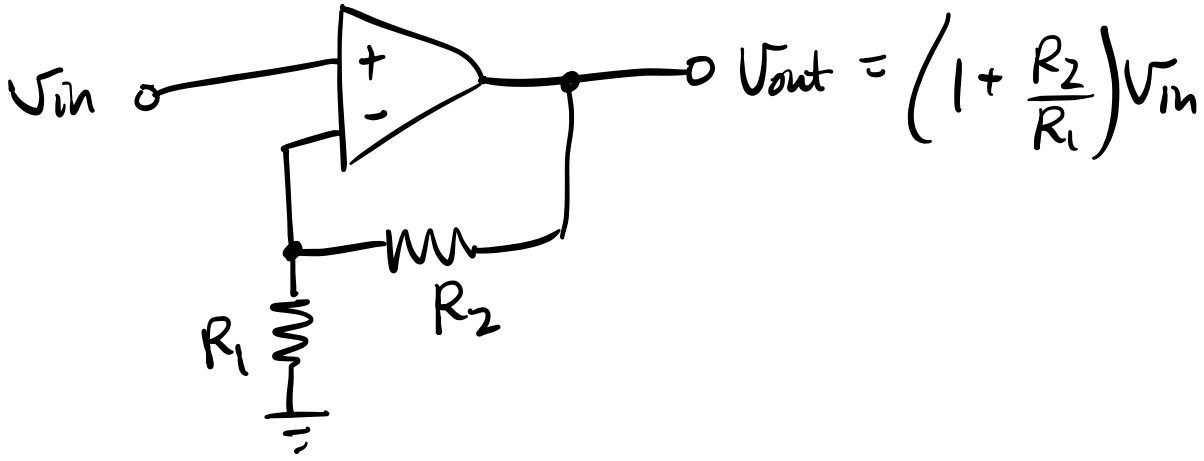
PHYS 231 – Nov. 6, 2023

Last Time:

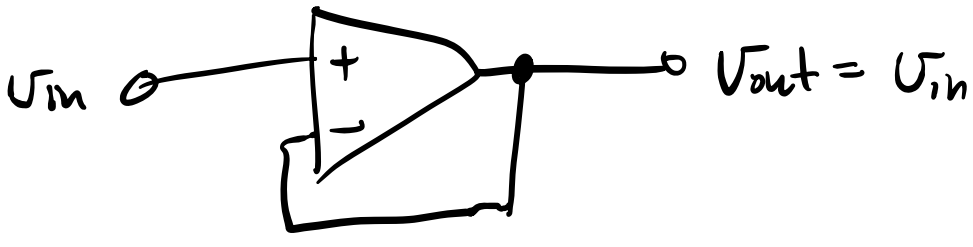
Inverting Amplifier:



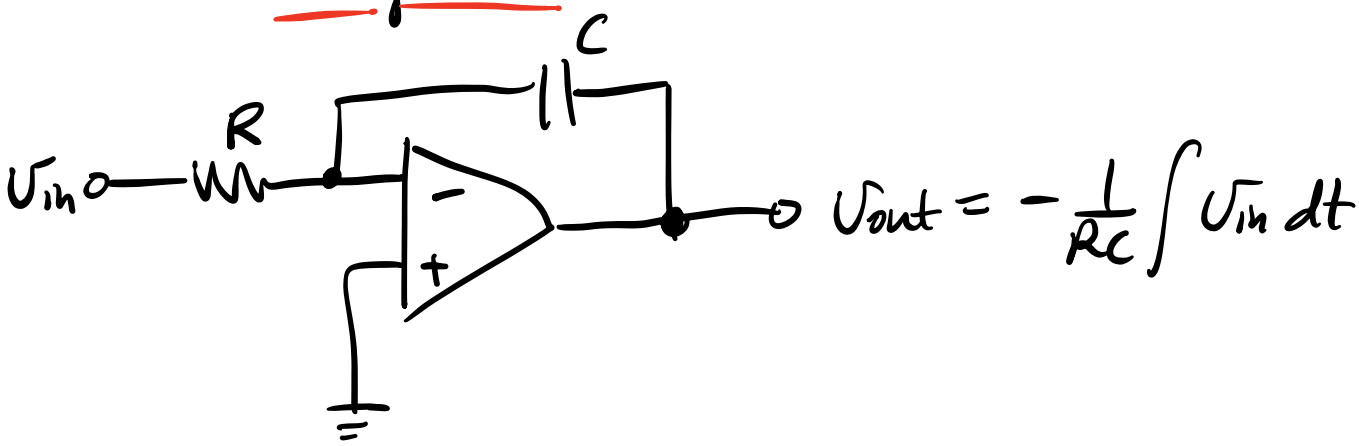
Non-inverting amplifier:



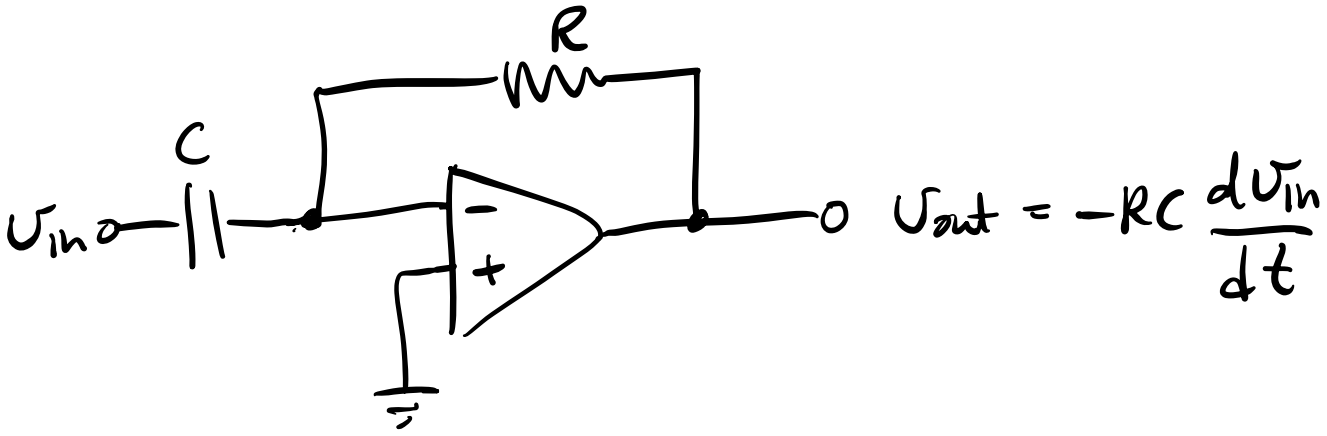
Buffer ($R_1 \to \infty$, $R_2 \to 0$)



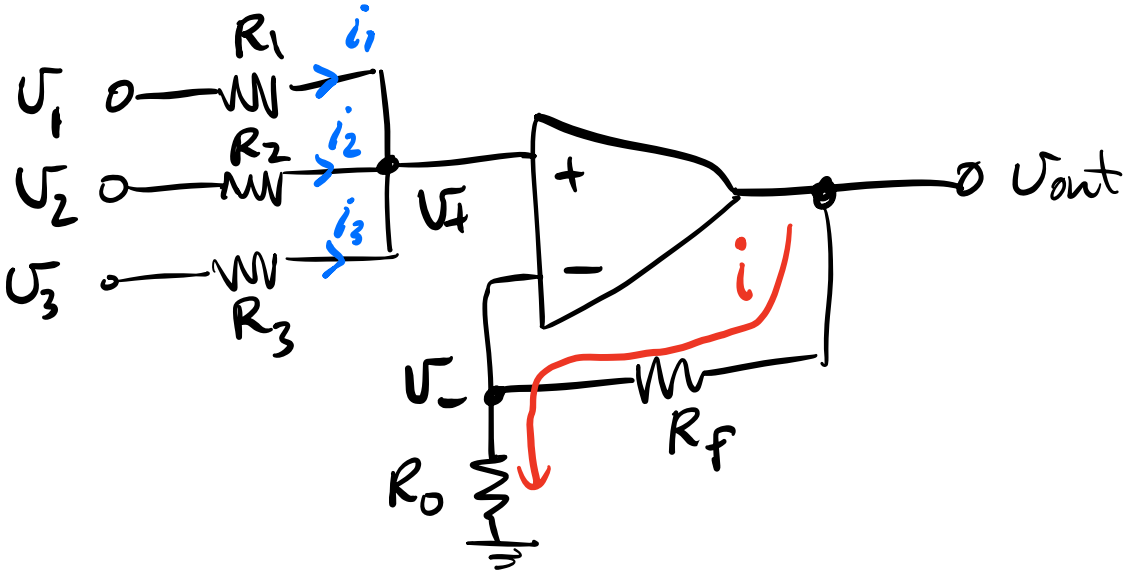
Integrator



Differentiator (can show that...)



Today: Summing Circuit



Golden rule #1: $i_- = i_+ = 0$

No current into/out of inputs.

- All current through R_f goes to gnd via R_0.
- $\underbrace{i_1 + i_2 + i_3}_{\text{current into node}} = \underbrace{0}_{\text{current out of node } (i_+ = 0)}$.

Voltage analysis start @ v_{out} & end @ gnd.

$$v_{out} - i(R_0 + R_f) = 0$$

$$\therefore i = \frac{v_{out}}{R_0 + R_f} \quad \|$$

$$\therefore v_- = iR_0 = v_{out}\frac{R_0}{R_0 + R_f} \quad \|$$

Know $v_- = v_+$ by 2nd G.R.

Start at V_1 & keep track of voltage changes to V_+.

$$V_1 - i_1 R_1 = V_+$$

$$\therefore i_1 = \frac{V_1 - V_+}{R_1} \quad (1)$$

Likewise, find $i_2 = \frac{V_2 - V_+}{R_2}$ (2)

$$i_3 = \frac{V_3 - V_+}{R_3} \quad (3)$$

Sub (1), (2), & (3) into jcn rule $i_1 + i_2 + i_3 = 0$.

$$\frac{V_1 - V_+}{R_1} + \frac{V_2 - V_+}{R_2} + \frac{V_3 - V_+}{R_3} = 0$$

$$\therefore \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) - V_+\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) = 0$$

$$\therefore \quad V_+ = \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)^{-1}$$

Finally, sub $V_+ = V_{out}\,\dfrac{R_0}{R_0+R_f}$

$$V_{out}\,\frac{R_0}{R_0+R_f} = \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)^{-1}$$

$$\therefore V_{out} = \underbrace{\left(1 + \frac{R_f}{R_0}\right)}_{\text{gain factor}}\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)^{-1}$$

Weighted sum.

(Noninverting) Summing Amplifier

If $R_1 = R_2 = R_3 \equiv R$

then $V_{out} = \left(1 + \frac{R_f}{R_0}\right)\frac{1}{R}\left(V_1 + V_2 + V_3\right)\left(\frac{3}{R}\right)^{-1}$

$$\therefore \quad V_{out} = \left(1 + \frac{R_f}{R_0}\right) \frac{V_1 + V_2 + V_3}{3}$$

unweighted or equally-weighted sum.

If $R_f/R_0 = 2$, $\quad V_{out} = V_1 + V_2 + V_3$

Digital Electronics Introduction

In digital electronics, we will work with voltages that are in only one of two possible states: LO $\Rightarrow$ 0
HI $\rightarrow$ 1

Typically 0 V will correspond to (LO, 0)
5 V " " " (HI, 1)

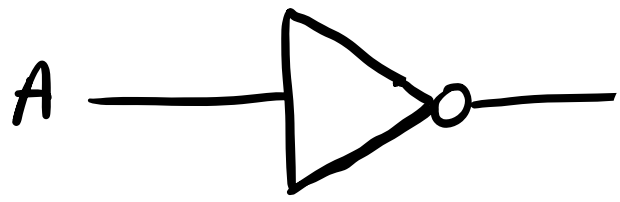
Digital signals are processed using logic gates.

Types of logic gates:

1. NOT (Inverter)

"NOT A"

one input



one output

(not an op amp)

Inverter Truth table

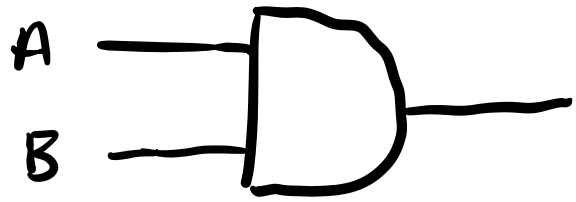
A	out = $\overline{A}$
0	1
1	0

In a truth table all possible input combs listed on left & corresponding outputs are listed on right.

Invertor simply changes the state of input to the opp. state at output.

2. AND

read as "A AND B"



two inputs

one output

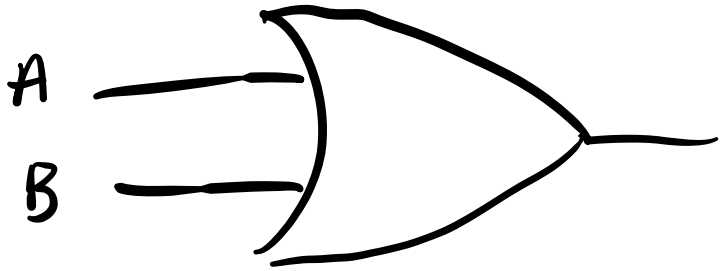
truth table

A	B	out = A • B
0	0	0
0	1	0
1	0	0
1	1	1

output is LO unless A AND B are HI.

3. OR gate

read as "A OR B"



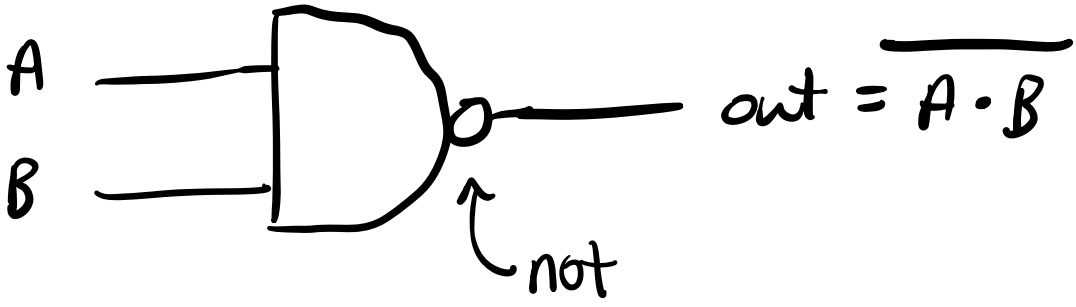
truth table

A	B	out = A + B
0	0	0
0	1	1
1	0	1
1	1	1

get out = HI if one or both of A & B are HI.

4. NOR (NOT AND)

read as "NOT A AND B" or "A NAND B".

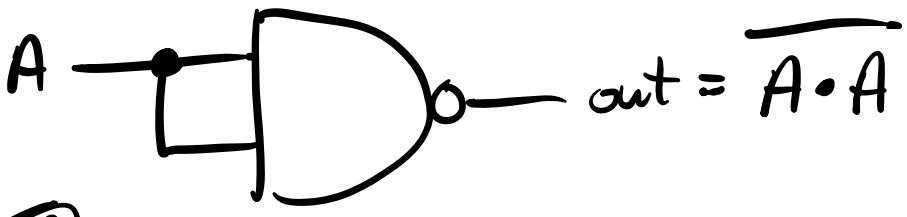


truth table

A	B	A · B	out = $\overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Note: All of the other logic gates can be constructed using only NANDs. NAND has become the industry standard.

Eg. Try connecting A & B inputs of a NAND

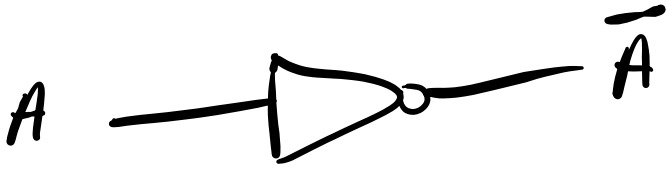


A	A	A·A
0	0	0
1	1	1

What's $A \cdot A = A$

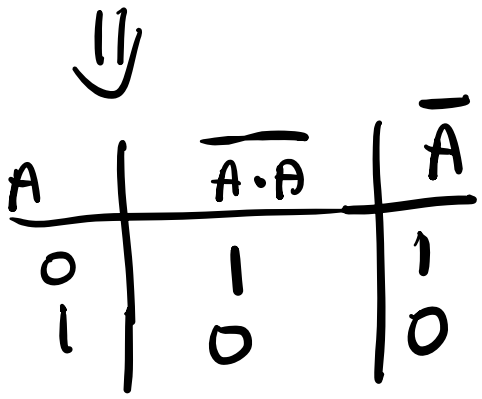
$\therefore \overline{A \cdot A} = \overline{A}$ → inverter

equiv



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

not allowed for A = B



A	$\overline{A \cdot A}$	$\bar{A}$
0	1	1
1	0	0

Exercise for the student.

Design an OR gate using only NANDs

→ need 3 NANDs to make an OR

→ Exp. #7 on Thursday.